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Vertical wrap-gated nanowire transistors

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Abstract
We present a process for fabricating a field-effect transistor based on vertically standing InAs nanowires and demonstrate initial device characteristics. The wires are grown by chemical beam epitaxy at lithographically defined locations. Wrap gates are formed around the base of the wires through a number of deposition and etch steps. The fabrication is based on standard III–V processing and includes no random elements or single nanowire manipulation.

1. Introduction

Electronics based on semiconductor nanowires is a rapidly evolving field. There is impressive progress in the methods used to fabricate nanowires, and a large number of semiconductor materials can now be used. Techniques ranging from solution-based synthesis [1] and laser ablation [2] to more traditional epitaxial growth [3] are used. The performance of discrete devices is also getting better and can in certain aspects be comparable to silicon CMOS [4]. However, one aspect that is still lagging behind is the scalability of the fabrication processes currently used. In order for the technology to be useful it is important that the fabrication methods are reliable and suitable for integration. In this paper, we demonstrate a device design that points to a possible way forward in this respect. The transistor fabrication presented is based exclusively on standard parallel III–V processes except for the first step when the patterning for the nanowire growth is done; this is done by electron beam lithography (EBL). This EBL processing step could be replaced by a nanoimprint lithography (NIL) patterning step [5]. The gate length is controlled by the etch back of an organic film and is $\sim$1 μm in the present device generation. The drive current is determined by the number of nanowires that are used as the channel, and can be chosen arbitrarily. We use InAs as the semiconductor material, which provides a high electron mobility and the possibility of obtaining high speed and low power operation.

The nanowires are grown on an InAs (111)B surface by chemical beam epitaxy (CBE) (figure 1). Gold discs, defined by electron beam lithography (EBL), are used as catalysts for growth [6]. The diameter of the nanowires is controlled via the diameter of the gold discs, and can be chosen between $\sim$40 nm and 200 nm. The length of the wires is controlled by the growth time and can varied between 0 and 5 μm. Even longer wires can be grown, but for the purpose of transistor fabrication this is not desirable. Wires only grow at the pre-defined locations, and the two-dimensional growth rate is low.

The transistors are fabricated using a matrix of nanowires as channels, typically 11 $\times$ 11 wires. This is to increase the drive current and the signal-to-noise ratio in the electrical measurements. The diameter of the wires is designed to be 80 nm in this study. In the present layout, the substrate acts as the source contact while the drain contact is formed at the top of the wires. In figure 2 a schematic view of the transistor, before the drain contact is formed, can be seen. The gate wraps around the base of the wire, and it is separated both from the substrate and the wire by an insulating layer of SiN_x. The drain contact is formed either by an air-bridge to the top of the wire or by a contact insulated by SiN_x.

2. Fabrication

Each transistor channel is composed of a matrix of 11 $\times$ 11 InAs nanowires grown with a pitch of 1 μm. The length of the wires is $\sim$4 μm. The pitch can be chosen smaller than 1 μm.

The first process step after the epitaxial growth is deposition of the insulating gate dielectric. We use 50 nm SiN_x deposited at room temperature in an ICP RIE from Oxford

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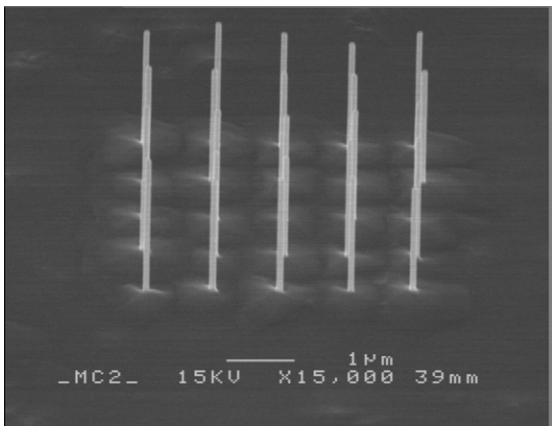

Figure 1. InAs nanowires grown by chemical beam epitaxy.

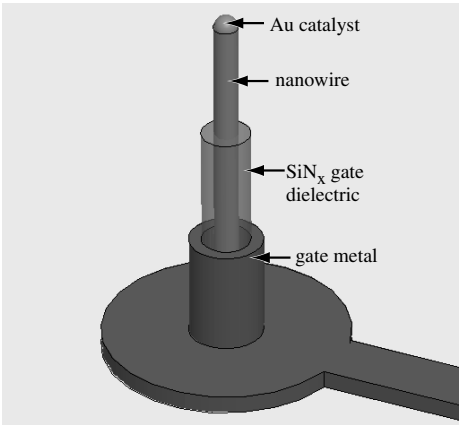

Figure 2. Schematic layout of the transistor. The gate wraps around the base of the wire, and is isolated from the nanowire by a layer of SiN_x. Only one wire is shown in the schematic diagram, while a matrix of wires is used in our actual devices.

(Oxford Plasmalab System 100). We use SiH_4 (8 sccm) and N_2 (20 sccm) as reactive gases and Ar (50 sccm) to stabilize the process; the ICP power is 100 W. The SiN_x deposited in this way shows good insulating properties and the DC characteristics of the transistor can be measured. The material and interface must, however, be further optimized for high performance devices.

The next step is depositing gate metal, which is done by sputtering of titanium. We use argon DC sputtering in a Balzers PLS 550. After this sputtering step, the whole chip is covered with SiN_x and titanium. At this stage, optical lithography and wet etching are used to define the gate pad, the gate finger and the drain pad. Diluted HF ($HF:H_2O$, 1:100) is used to remove the unwanted titanium. To have the gate wrapping only around the base of the wire we spin on a resist (AZ4533) and etch it back to a thickness of 1 μm. Thereafter the titanium is etched away from the upper part of the wires using $HF:H_2O$, 1:100. This leaves us with the situation illustrated in figure 3, where the SiN_x is still covering the whole wire. The gate length is controlled by the etch back of the resist and is 1 μm.

Before the drain contact is formed the chip is once again covered in 150 nm SiN_x; this will provide mechanical stability and ensure isolation between the gate and drain (figure 4).

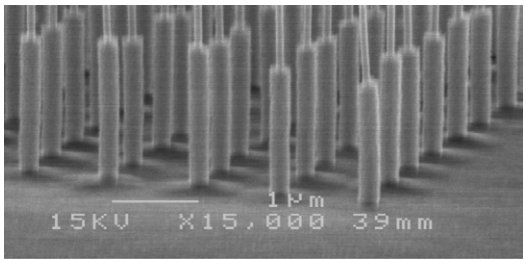

Figure 3. SEM image showing nanowires after the wrap gate is formed. The gate length is $\sim$1 μm.

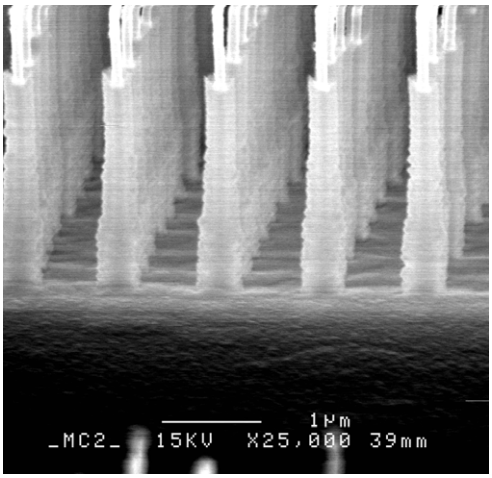

Figure 4. The nanowire channels after the gate is formed and a protective layer of SiN_x has been deposited. The protective SiN_x layer has been etched away from the uppermost part of the wires to allow for drain contact formation.

We use two different methods to form the drain contact: either an air-bridge [7, 8] (figure 5) or a contact deposited directly on the protective SiN_x (figure 6). The air-bridge technique has the advantage of lower parasitic capacitance between the drain and source/gate, which might prove valuable in applications where transistor speed is important. On the other hand, the technology is more complicated and the number of process steps that are needed is increased. In both approaches the drain contact wraps around $\sim$1 μm of the wires, which will reduce the contact resistance since the contact area is large.

The air-bridge consists of electroplated Au with a thin contact layer of Ti to form a low resistance contact, without annealing. The fabrication process includes the following steps, starting at the stage pictured in figure 4:

- Spin on photoresist AZ4533 and expose and develop to reveal the gate and drain pad.
- Etch back the remaining resist layer to 2 μm thickness.
- Remove the SiN_x from the top of the wires and from the pads in an NF_3 plasma etch (Oxford Plasmalab System 100).
- Deposit a seed layer for electroplating consisting of 100 nm Ti and 50 nm Au (sputtering in a Balzers PLS 550).
- Define the drain contact pad, air-bridge and gate contact pad with optical lithography.

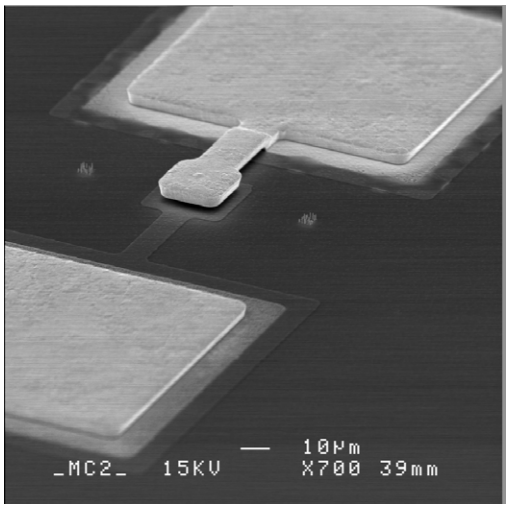

Figure 5. SEM image of the completed device with the air-bridge contacted drain.

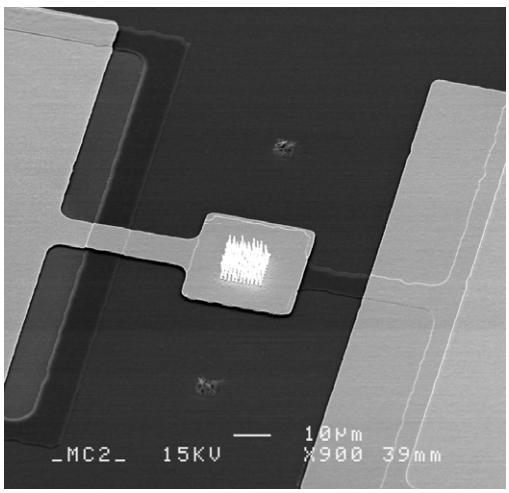

Figure 6. SEM image of the completed device showing the gate and drain fingers and the nanowire channels.

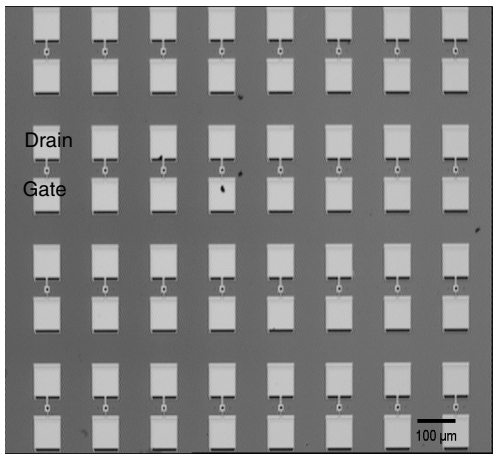

Figure 7. Optical top-view image of 32 completed devices.

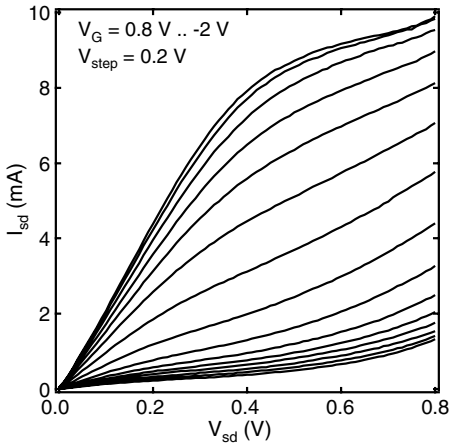

Figure 8. I–V characteristics of a transistor with ∼120 nanowire channels. The measurement is done in the common source configuration with the substrate acting as the source. The curves are recorded in one sweep from positive to negative gate voltage to avoid the hysteresis that is otherwise present.

- Electroplate Au to a thickness of ∼5 μm.
- Remove the upper photoresist layer and etch away the seed layer in a wet etch (Gullets from Sunchem AB and HF:H_2O, 1:100).
- Remove the remaining resist layer in O_2 plasma and acetone.

In the second approach where the contact is deposited directly onto the protective SiN_x the process flow is the following, starting at the stage pictured in figure 4:

- Spin on photoresist AZ4533 and expose and develop to reveal the gate and drain pad.
- Etch back the remaining photoresist to 2 μm thickness.
- Remove the SiN_x from the top of the wires in an NF_3 plasma etch (Oxford Plasmalab System 100).
- Remove the remaining resist in acetone and O_2 plasma.
- Deposit metal for the drain contact consisting of 100 nm Ti and 200 nm Au (sputtering in a Balzers PLS 550).
- Define the drain contact pad, air-bridge and gate contact pad with optical lithography.
- Etch away the unwanted metal in a wet etch (Gullets from Sunchem AB and HF:H_2O, 1:100).
- Remove the photoresist layer in acetone.

In figure 7 an optical image of a part of a completed chip can be seen. As the substrate is a common source for all the transistors, this layout is for characterization of individual devices only.

3. Results and discussion

The I–V characteristics of a transistor with ∼120 nanowire channels, giving a total cross-section area of the channel of 0.6 μm^2, is shown in figure 8. A transconductance of 6 mS and a drive current of ∼6 mA are measured at zero gate voltage. This corresponds to a current density of 50 μA per nanowire. The gate leakage current is below 1 nA and is

probably dominated by leakage from the large area gate pad to the substrate. The transistor does not pinch off correctly, as can be seen in figure 8. This is due to leakage between the substrate and the drain contact pad. Hysteresis effects can be seen in the output characteristics and the transfer characteristics; this may be due to charge traps at the interface between the InAs channel and the SiN_x gate dielectric or to imperfections in the dielectric layer.

4. Conclusions

In conclusion, we have demonstrated a vertical wrap-gated nanowire FET. The design is based on a matrix of lithographically defined, bottom-up fabricated, InAs nanowires that act as the channel in the transistor. A novel processing scheme, based almost exclusively on parallel processes, suggests that batch fabrication is feasible. Encouraging electrical data are demonstrated.

Acknowledgment

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